INTEGRATED VOICE-OVER-INTERNET PROTOCOL PROCESSOR

Related Applications

This application claims the benefit of provisional Application No. 60/153,762, filed September 13, 1999, the benefit of which is hereby claimed under 35 U.S.C. § 119.

Field of the Invention

The present invention relates to communication systems in general, and in particular to Voice-over-Internet Protocol (IP) communication systems.

Background of the Invention

As computer networks become more prevalent and powerful, the boundaries between traditional telephony and data communication become increasingly blurred. For example, the Internet is a global network of computers wherein data is transmitted from a source to a destination as a series of individually addressed packets. Such packets are most often used to carry computer data. However, it is also possible to transmit real time voice data over a packetized network, provided that proper compression techniques are used and the speed of the network is fast enough to avoid producing noticeable delay. When operating correctly, voice data transmitted over the Internet has nearly the same quality as voice data transmitted over conventional telephone lines.

One advantage of using an Internet protocol (IP) network to carry both computer and voice data in an area is that only a single set of wiring is needed. This is particularly advantageous for large businesses where the cost of installing the wiring for both data and telecommunications networks is considerable.

Most voice over IP network telephones are controlled by a network processor that performs the functions of data compression and encoding as well as transmitting and receiving data from the computer network. In the past, such network processors had limited ability to interface with other peripherals, thereby requiring a number of other electronic sub-systems to be provided in order to construct a functioning voice over IP telephone. To increase the number of potential applications for such processors and to reduce the cost of the systems that employ them, there is a need for a network processor having integrated peripheral interfaces.

Summary of the Invention

The present invention is a voice over IP network processor that can be used for transmitting both computer and voice data over a packetized computer network. The network processor includes integrated circuitry that connects the processor to a variety of peripherals. Specifically, the network processor includes one or more integrated universal serial bus (USB) ports, IEEE 802.3 media access controllers (MACs), a repeater and integrated PCM HDLC ports that allow peripherals such as A/D and D/A converters to be easily interfaced with the processor. The peripheral interfaces are integrated into the processor through a flexible peripheral interconnect (FPI) bus.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a block diagram of an Internet protocol phone in accordance with the present invention; and

FIGURE 2 is a block diagram of a Voice-over-Internet Protocol processor including integrated USB ports, media access controllers, repeater ports and a pair of integrated pulse code modulation ports in accordance with the present invention.

Detailed Description of the Preferred Embodiment

FIGURE 1 is a block diagram of a Voice-over-Internet Protocol (IP) telephone system constructed in accordance with the present invention. The telephone system 10 comprises a network processor 12 that performs a variety of functions including assembling a digital voice signal into a series of packets and transmitting and receiving packets over a local area network 13.

The local area network 13 may be coupled to a wide area network such as the Internet, through a gateway (not shown). The telephone system 10 also includes a microphone 14a, speaker 14b and handset 14c that are connected to the network processor 12 through a digital-to-analog/analog-to-digital (DA/AD) converter 22. The DA/AD converter 22 is connected to the network processor 12 via an integrated pulse code modulation (PCM) port 24 that is described in further detail below. Each of the PCM ports can handle up to 30 time slots with each slot capable of handling a 64K bit/sec voice channel. The PCM ports therefore serve as the interface between the internal hardware of the IP processor and an external peripheral. In addition to transmitting and receiving voice data, the telephone system also transmits and receives data from a workstation 18 that is connected to the network processor 12 through an Ethernet port 26. A second Ethernet port 28 is used to connect the network processor to the local area network 13.

A keypad 30 is interfaced with the network processor 12 to allow a user to dial telephone numbers and an LCD display 32 is provided so that a user can see the information entered on the keypad. Finally, the telephone system 10 includes a memory unit 34 to store programs and other data required by the network processor 12.

FIGURE 2 is a block diagram of the network processor 12, the details of which are more fully described in the specification titled "Harrier-VT" as attached as Appendix A. Although the presently preferred embodiment is constructed around the TRICORE and Harrier processors available from Infineon Technologies of San Jose, California, it will be appreciated that any computing architecture having the functionality described could be substituted.

Integrated USB Port

A USB port 21 is integrated on the same circuit as the network processor 12 as described in the specification entitled "Universal Serial Bus Device Controller 1.1" attached as Appendix B. The USB port 21 provides a simple interface to other USB compatible devices without having to provide external interfacing circuitry.

Integrated IEEE 802.3 MACs and Repeater

To connect the network processor directly to a local area network, the processor 12 includes a pair of IEEE 802.3 media access controllers and a repeater in accordance with the IEEE standard.

Each of the USB ports, 802.3 MACs and the PCM ports are connected to a flexible peripheral interconnect bus 34 that is described in the specifications entitled

"Flexible Peripherals Interconnect Bus Version 3.2" and "BPI Specification Draft Version 0.9" as attached as Appendices C and D, respectively.

Integrated PCM Ports

As discussed above, to provide a convenient interface to the DA/AD converter 22, the network processor 12 includes a pair of integrated PCM ports 24. The PCM ports comprise a number of sub-components including a data management unit transmit block 24a and data management receive block 24b that are described in the attached specification entitled "Macro Specification DMUT Version 2.2" and "Macro Specification DMUR Version 2.2" attached as Appendices E and F, respectively.

In addition, the PCM ports include a transmit and receive buffer 24c and 24d that are described in the specifications entitled "Macro Specification TB Version 2.1", "Macro Specification TB data sheet" and "Receive Buffer V2.1" attached as Appendices G, H and I, respectively.

Also included in the PCM ports 24 are a protocol machine transmit and receive blocks 24e and 24f that are described in the specifications entitled "Protocol Machine Transmit Version 2.2" and "Macro Specification PMR Version 2.1" attached as Appendices J and K, respectively.

A time slot assignee receive and transmit blocks 24g and 24h are included in the PCM ports 24 and are described in the specifications entitled "Timeslot Assigner Receive V2.2.1" and "Timeslot Assigner Transmit V2.2.1" attached as Appendices L and M, respectively.

The PCM port 24 also includes a receive/transmit port interface block 24i, 24j that are described in the specification entitled "Receive/Transmit Port Interface V2.3.1" attached as Appendix N.

A data management transmit and receive blocks 24a and 24b are connected to the FPI bus 34 through a master/slave interface that is described in the specification entitled "Platform Concept: SMIF Specification Version 1.0" attached as Appendix O.

The remaining components of the PCM port 24 are connected to the FPI bus 34 through a BPI interface as described in "BPI Specification Draft Version 0.9" attached as Appendix P.

As can be seen from the above description, the present invention is a single-chip voice over IP network processor having integrated interface ports that

allow the processor to be easily coupled to a variety of external components and peripherals.